REMARKS

Applicants respectfully request further examination and reconsideration in view of the amendments above and the comments set forth fully below. Claims 1-31 were previously pending. Within the Office Action, Claims 1-4, 7-11, 14-19, 22-27, 30 and 31 have been rejected, and Claims 5, 6, 12, 13, 20, 21, 28 and 29 have been objected to. Accordingly, Claims 1-31 are now pending.

Rejections Under 35 U.S.C. § 103(a)

Within the Office Action, Claims 1-3, 7-10, 14, 16-18, 22-26 and 30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,847,365 to Miller et al. (hereinafter "Miller") in view of U.S. Patent No. 4,725,973 to Matsuura et al. (hereinafter "Matsuura"). The Applicants respectfully disagree with this rejection.

Miller teaches a media processing system which includes DRAM for storing digital data, including compressed video data, a processor, a decoder to generate full motion video pixel data, a system for sharing the DRAM between the processor and the decoder and a system for producing a full motion video signal from the full motion video pixel data. Miller teaches that the media processing system has the processing elements connected together in parallel. [Miller, Abstract] Miller also teaches the invention is not limited to any particular number of processing elements. [Miller, col. 7, lines 3-10] However, Miller does not teach configuring a plurality of processing elements into a two-dimensional array of processing elements. Simply because there are "any particular number of MPEs" within Miller does not mean the processing elements are configured in a two-dimensional array. Specifically, Figure 3 of Miller clearly shows MPE0, MPE1, MPE2 and MPE3 in a one-dimensional row, not in a two-dimensional array. Furthermore, Miller also does not teach, explicitly or implicitly, a plurality of block registers included in each processing element as is explained further below.

Matsuura teaches a vector processor for executing vector instructions which comprises a plurality of vector registers and a plurality of pipeline arithmetic logic units. [Matsuura, Abstract] Matsuura also teaches two element series are simultaneously read from the vector register array and are concurrently processed by two arithmetic logic units. [Matsuura, col. 3, lines 19-21]

Matsuura does not teach a plurality of block registers included in each processing element. Matsuura also does not teach configuring a plurality of processing elements into a two-dimensional array of processing elements.

Neither Miller, Matsuura nor their combination teach a plurality of block registers included in each processing element. Further, neither Miller, Matsuura nor their combination teach configuring a plurality of processing elements into a two-dimensional array of processing elements.

In contrast to Miller, Matsuura and their combination, the present invention discloses a video platform architecture which provides video processing using parallel vector processing. The video platform architecture includes a plurality of video processing modules, each module including a plurality of processing elements (PEs). Each PE provides parallel vector processing. Specifically, all elements of one or two source vector registers in each PE are read simultaneously, the read elements are processed by a set of arithmetic-logical units (ALUs), and all results are written back to one of the vector registers, in one PE cycle. To provide such parallel vector processing capabilities, the datapath of each PE is built as a set of identical PE processing slices, each of which includes an integer arithmetic-logical unit (ALU), a vector register bank and a block register bank. [Present Specification, Abstract] Furthermore, the present invention discloses a two-dimensional array of processing elements. [Present Specification, page 10, lines 3-5 and accompanying Figure 2] As described above, neither Miller, Matsuura nor their combination teach a plurality of block registers. As also described above, neither Miller, Matsuura nor their combination teach configuring a plurality of processing elements into a two-dimensional array of processing elements.

Within the Office Action, it is stated that Miller implicitly discloses a plurality of block registers which function similar to vector registers. Applicants respectfully disagree. No where in Miller are block registers even remotely suggested. Furthermore, it appears that it is the contention of the Office Action, that block registers and vector registers are the same. Applicants respectfully disagree. Throughout the Present Specification, clear distinctions are made between the block registers and the vector registers. "Block registers serve as an intermediate register level allowing the exchange of data between the PE and the block load/store unit, or between two

PEs, to proceed in parallel with operations on vector registers inside PEs." [Present Specification, page 11, lines 1-3] "In order to store PE results in memory, the results from the PE's vector register are first moved to any of the PE's block registers..." [Present Specification, page 14, lines 1-2] "At the step 602, a video stream is configured into data blocks. At the step 604, the data blocks are loaded into the plurality of block registers within each processing element. At the step 606, the data blocks are loaded from the plurality of block registers to the plurality of vector registers." [Present Specification, page 16, lines 21-24] It is further taught within the present specification that

> a video stream is received by a video platform architecture which configures the video stream into data blocks and sends the data blocks to an array of processing elements. Each data block is configured according to I columns and J rows of data elements. The processing elements are configured into a two-dimensional array, each processing element including a plurality of vector registers, a plurality of block registers, a plurality of scalar registers, and a plurality of arithmetic logic units (ALUs). Each block register and each vector register are configured to hold one data block. Within each processing element, identical data paths are configured which essentially divide the processing element into processing slices. Each processing slice includes a vector register bank, a block register bank, and an arithmetic logic unit. Each block register bank holds all I elements of row J for each IxJ data block for all block registers in the processing element. Data blocks are processed while in the vector registers. As such, to process the data blocks, the data blocks are loaded into the plurality of vector registers from the plurality of block registers. [Present Specification, page 16, line 30 through page 17, line 10]

Clearly, there are significant differences between vector registers and block registers, and it is not appropriate to assume that they are the same. Since, they are not the same, it is incorrect to conclude that Miller implicitly discloses a plurality of block registers.

The independent Claim 1 is directed to a method of processing video. The method of Claim 1 comprises configuring a plurality of processing elements into a two-dimensional array of processing elements such that each processing element includes a plurality of vector registers, a plurality of block registers, a plurality of scalar registers, and a plurality of arithmetic logic units, wherein a data path of each processing element includes a set of processing element slices each coupled to one arithmetic logic unit such that each arithmetic logic unit receives a specified

portion of each vector register as input, configuring a video stream into data blocks, loading the data blocks into the plurality of vector registers within each processing element, reading the specified portions of each vector register by each of the corresponding arithmetic logic units within all processing elements simultaneously and processing the read portions by the arithmetic logic units such that the data blocks from the plurality of vector registers are processed in parallel. As described above, neither Miller, Matsuura nor their combination teach a plurality of block registers included in each processing element. As also described above, neither Miller, Matsuura nor their combination teach configuring a plurality of processing elements into a two-dimensional array of processing elements. For at least these reasons, the independent Claim 1 is allowable over the teachings of Miller, Matsuura and their combination.

Claims 2, 3, 7 and 8 are all dependent on the independent Claim 1. As discussed above, the independent Claim 1 is allowable over the teachings of Miller, Matsuura and their combination. Accordingly, Claims 2, 3, 7 and 8 are all also allowable as being dependent on an allowable base claim.

The independent Claim 9 is directed to an apparatus to process video. The apparatus of Claim 9 comprises a main memory and a two-dimensional array of processing elements, wherein each processing element includes a plurality of vector registers, a plurality of block registers, a plurality of scalar registers, and a plurality of arithmetic logic units, further wherein a data path of each processing element includes a set of processing element slices each coupled to one arithmetic logic unit such that each arithmetic logic unit receives a specified portion of each vector register as input, wherein video data is received by the main memory and configured as data blocks, the data blocks are loaded into the plurality of vector registers within each processing element, specified portions of each vector register are read by each of the corresponding arithmetic logic units simultaneously within all processing elements, the read portions are processed by the arithmetic logic units such that the data blocks from the plurality of vector registers are processed in parallel, and the results of the processing performed by the arithmetic logic units are written to the plurality of vector registers. As described above, neither Miller, Matsuura nor their combination teach a plurality of block registers included in each processing element. As also described above, neither Miller, Matsuura nor their combination

teach a two-dimensional array of processing elements. For at least these reasons, the independent Claim 9 is allowable over the teachings of Miller, Matsuura and their combination.

Claims 10 and 14 are both dependent on the independent Claim 9. As discussed above, the independent Claim 9 is allowable over the teachings of Miller, Matsuura and their combination. Accordingly, Claims 10 and 14 are both also allowable as being dependent on an allowable base claim.

The independent Claim 16 is directed to an apparatus to process video. The apparatus of Claim 16 comprises means for configuring a plurality of processing elements into a two-dimensional array of processing elements such that each processing element includes a plurality of vector registers, a plurality of block registers, a plurality of scalar registers, and a plurality of arithmetic logic units, wherein a data path of each processing element includes a set of processing element slices each coupled to one arithmetic logic unit such that each arithmetic logic unit receives a specified portion of each vector register as input, means for configuring a video stream into data blocks coupled to the means for configuring a plurality of processing elements, means for loading the data blocks into the plurality of vector registers within each processing element, the means for loading coupled to the means for configuring the video stream, means for reading the specified portions of each vector register by each of the corresponding arithmetic logic units within all processing elements simultaneously, the means for reading coupled to the means for loading and means for processing the read portions by the arithmetic logic units such that the data blocks from the plurality of vector registers is processed in parallel, the means for processing coupled to the means for reading. As described above, neither Miller, Matsuura nor their combination teach a plurality of block registers included in each processing element. As also described above, neither Miller, Matsuura nor their combination teach means for configuring a plurality of processing elements into a two-dimensional array of processing elements. For at least these reasons, the independent Claim 16 is allowable over the teachings of Miller, Matsuura and their combination.

Claims 17, 18, 22 and 23 are all dependent on the independent Claim 16. As discussed above, the independent Claim 16 is allowable over the teachings of Miller, Matsuura and their

combination. Accordingly, Claims 17, 18, 22 and 23 are all also allowable as being dependent on an allowable base claim.

The independent Claim 24 is directed to an apparatus to process video. The apparatus of Claim 24 comprises a two-dimensional array of processing elements, wherein each processing element includes a plurality of vector registers, a plurality of block registers, a plurality of scalar registers, and a plurality of arithmetic logic units, further wherein a data path of each processing element includes a set of processing element slices each coupled to one arithmetic logic unit such that each arithmetic logic unit receives a specified portion of each vector register as input. As described above, neither Miller, Matsuura nor their combination teach a plurality of block registers included in each processing element. As also described above, neither Miller, Matsuura nor their combination teach a two-dimensional array of processing elements. For at least these reasons, the independent Claim 24 is allowable over the teachings of Miller, Matsuura and their combination.

Claims 25, 26 and 30 are all dependent on the independent Claim 24. As discussed above, the independent Claim 24 is allowable over the teachings of Miller, Matsuura and their combination. Accordingly, Claims 25, 26 and 30 are all also allowable as being dependent on an allowable base claim.

Within the Office Action, Claims 4, 11, 19 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miller in view of Matsuura and further in view of U.S. Patent No. 5,226,171 to Hall et al. (hereinafter "Hall"). Applicants respectfully disagree.

Claim 4 is dependent on the independent Claim 1. Claim 11 is dependent on the independent Claim 9. Claim 19 is dependent on the independent Claim 16. Claim 27 is dependent on the independent Claim 24. As discussed above, the independent Claims 1, 9, 16 and 24 are all allowable over the teachings of Miller, Matsuura and their combination. Accordingly, Claims 4, 11, 19 and 27 are all also allowable as being dependent on allowable base claims.

Within the Office Action, Claims 15 and 31 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Miller in view of Matsuura and further in view of "*A bit-serial VLSI*

array processing chip for image processing" by Heaton et al. (hereinafter "Heaton"). Applicants respectfully disagree.

Claim 15 is dependent on the independent Claim 9, Claim 31 is dependent on the independent Claim 24. As discussed above, the independent Claims 9 and 24 are both allowable over the teachings of Miller, Matsuura and their combination. Accordingly, Claims 9 and 31 are both also allowable as being dependent on allowable base claims.

Within the Office Action, it is stated that Claims 5, 6, 12, 13, 20, 21, 28 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 5 and 6 are dependent on the independent Claim 1. Claims 12 and 13 are dependent on the independent Claim 9. Claims 20 and 21 are dependent on the independent Claim 16. Claims 28 and 29 are dependent on the independent Claim 24. As discussed above, the independent Claims 1, 9, 16 and 24 are all allowable over the teachings of Miller, Matsuura and their combination. Accordingly, Claims 5, 6, 12, 13, 20, 21, 28 and 29 are all also allowable as being dependent on allowable base claims.

For the reasons given above, Applicants respectfully submit that the claims are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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